Claims

1. A method for enhancing the fabrication process of a self-aligned contact (SAC) structure, the method comprising:

forming a transistor structure on a surface of a substrate;

forming a dielectric layer directly over the surface of the substrate without forming an etch stop layer thereon;

plasma etching a contact hole through the dielectric layer in a plasma processing chamber;

monitoring a bias compensation voltage of the plasma processing chamber during the plasma etching; and

discontinuing the plasma etch process upon detecting an endpoint signaling change in the bias compensation voltage.

2. A method for enhancing the fabrication process of a self-aligned contact (SAC) structure as recited in claim 1, wherein the endpoint signaling change in the bias compensation voltage is detected when a portion of the surface of the substrate underlying the contact hole is substantially exposed.

3. A method for enhancing the fabrication process of a self-aligned contact (SAC) structure as recited in claim 1, wherein the endpoint signaling change is an expected step increase in the bias compensation voltage.

4. A method for enhancing the fabrication process of a self-aligned contact (SAC) structure as recited in claim 1, wherein forming the transistor structure on the surface of the substrate includes,

forming a gate structure over the surface of the substrate;

forming spacers along sidewalls of the gate structure; and

forming source/drain diffusion regions into the surface of the substrate, the source/drain diffusion regions being defined substantially outside of the spacers formed along sidewalls of the gate structure.

5. A method for enhancing the fabrication process of a self-aligned contact (SAC) structure as recited in claim 1, wherein the dielectric layer is an interlevel dielectric (ILD) layer.

6. A method for enhancing the fabrication process of a self-aligned contact (SAC), the method comprising:

forming a transistor structure on a substrate, the transistor structure including a gate structure formed over a first surface of the substrate;

forming spacers along sidewalls of the gate structure;

forming source/drain diffusion regions into the first surface of the substrate, the source/drain diffusion regions being defined substantially outside of the spacers formed along sidewalls of the gate structure;

forming an interlevel dielectric (ILD) layer directly over the first surface of the substrate without forming a stop layer, such that the ILD layer overlies the gate structure, the spacers, and the first surface of the substrate;

forming a contact hole and a via hole in the ILD layer implementing a plasma etching process such that the contact hole is defined to a top layer of the gate structure and the via hole is defined to the source/drain diffusion regions;

monitoring a bias compensation voltage during the plasma etching process; and

discontinuing the plasma etching process when an endpoint signaling change in the bias compensation voltage is detected.

7. A method for enhancing the fabrication process of a self-aligned contact (SAC) as recited in claim 6, wherein the endpoint signaling change in the bias compensation voltage is detected when a portion of the top layer of the gate structure underlying the contact hole and a portion of the source/drain diffusion regions underlying the via hole are substantially exposed.

8. A method for enhancing the fabrication process of a self-aligned contact (SAC) as recited in claim 6, wherein the gate structure includes,

a gate oxide formed over the first surface of the substrate; and

a polysilicon gate formed over the gate oxide.

9. A method for enhancing the fabrication process of a self-aligned contact (SAC) as recited in claim 6, wherein forming the ILD layer over the first surface of the substrate includes,

depositing an oxide layer over the first surface of the substrate, the gate structure, and spacers;

depositing a tetraethylorthosilicate (TEOS) layer over the oxide layer; and

depositing an oxide layer over the TEOS layer.

10. A method for enhancing the fabrication process of a self-aligned contact (SAC) as recited in claim 6, wherein forming spacers along the sidewalls of the gate structure includes,

depositing a spacer layer over a first surface of the substrate and the gate structure; and

performing a plasma etching process configured to define spacers along the sidewalls of the gate structure.

11. A bias compensation self-aligned contact (SAC) etch endpoint detecting system, the system comprising:

an etch reactant chamber configured to include an electrostatic chuck (ESC), a top electrode, and a bottom electrode, the ESC configured to support a substrate having an interlevel dielectric (ILD) layer to be etched;

an ESC power supply coupled to the ESC, the ESC power supply being configured to function as a bias compensating power supply; and

a signal processing computer configured to monitor a bias compensation signal generated by the ESC power supply,

wherein an etch process to be carried out in the etch reactant chamber is configured to be discontinued when the bias compensation signal is determined to have a previously ascertained characteristic evidencing an etch endpoint of the ILD layer.

12. A bias compensation self-aligned contact (SAC) etch endpoint detecting system as recited in claim 11, wherein the previously ascertained characteristic evidencing the etch endpoint of the ILD layer is a change in a bias compensation voltage.

13. A bias compensation self-aligned contact (SAC) etch endpoint detecting system as recited in claim 12, wherein the bias compensation voltage configured to evidence the etch endpoint of the ILD layer correlates with the substantial removal of the exposed portions of the ILD layer and the substantial exposure of a portion of an underlying layer defined below the exposed portion of the ILD layer.

14. A bias compensation self-aligned contact (SAC) etch endpoint detecting system as recited in claim 12, wherein the previously ascertained characteristic evidencing the etch endpoint of the ILD layer is an expected step increase in the bias compensation voltage.

15. A bias compensation self-aligned contact (SAC) etch endpoint detecting system as recited in claim 12, Wherein the underlying layer is a source/drain diffusion region.

16. A method for accurately detecting a plasma etch endpoint of a self-aligned contact (SAC), the method comprising:

providing a substrate having a transistor structure on a surface of the substrate;

forming a dielectric layer directly over the surface of the substrate without forming an etch stop layer thereon;

inserting the substrate into a plasma etching chamber so as to plasma etch a contact hole into the dielectric layer;

introducing etchant gases into the plasma etching chamber;

powering up the plasma etching chamber, the powering up configured to strike a plasma so as to commence the plasma etching process;

monitoring a bias level of the plasma etching chamber during the plasma etching process; and

discontinuing the plasma etching process when an endpoint signaling change in the bias compensation voltage is detected.

17. A method for accurately detecting a plasma etch endpoint of a self-aligned contact (SAC) as recited in claim 16, wherein the endpoint signaling change in the bias compensation voltage is detected when a portion of the surface of the substrate underlying the contact hole is substantially exposed.

18. A method for accurately detecting a plasma etch endpoint of a self-aligned contact (SAC) as recited in claim 16, wherein the endpoint signaling change is an expected step increase in the bias compensation voltage.

19. A method for accurately detecting a plasma etch endpoint of a self-aligned contact (SAC) as recited in claim 16, wherein the dielectric layer is an interlevel dielectric (ILD) layer.

20. A method for accurately detecting a plasma etch endpoint of a self-aligned contact (SAC) as recited in claim 17, wherein the portion of the surface of the substrate underlying the contact hole is a gate structure.